Materials and Applications for Large Area Electronics: Solution-Based Approaches

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Contents

1. Introduction

In its most compelling forms, large area electronics addresses a range of applications outside those where monocrystalline Si and III−V integration are used, or it approaches those conventional applications with a uniquely advantageous performance benefit. Historically, much of the initial work in large area electronics has centered on displays and photovoltaics, as these are fundamentally area-intensive applications. However, over the last two decades, and especially in the last 10 years, the scope of applications envisioned for large area electronics has expanded dramatically. This research development area presently includes medical, wireless, sensing, flexible, and ultrathin applications. In some cases, new applications and device approaches, such as medical imaging arrays and flexible active matrix displays, have been a direct extension of previously developed amorphous silicon (a-Si) thin film transistor (TFT) active matrix backplanes for liquid crystal displays.[1,2] In other cases, new concepts have emerged such as integrated sensor technologies, printed radio frequency identification (RFID),

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and light-emissive flexible displays.[3] Of these applications, some have precursors in printed circuit board technology,

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integrated passive devices, and electroluminescent phosphor technologies. For others, it has been the development of broad, ubiquitous consumer product platforms and the general explosion of digital information available that have driven interest in thinner, more robust, and cheaper electronics capable of interacting with their environment on the macroscale.

For the purpose of this Review, large area electronics connotes either large device dimensions, significantly greater than current focus of conventional semiconductor technologies, and overall integrated devices or device arrays of tens of centimeters or even tens of meters. This is in contrast to the area-minimized, highly integrated Si chips of modern CMOS technology with extraordinary device densities and sizes from centimeters (PC microprocessors) containing as many as a billion transistors per chip, down to submillimeter, monolithic integrated circuits (RFID chips). The special challenge for large area electronics is to add high functionality to enable larger area electronics applications while limiting costs to deposit and pattern this functionality over large distances.

Table 1. Cost of Patterning Information over Larger Areas

technology	patterning	cost per bit	cost/area [$/cm^2]
newspaper	offset	$\$2 \times 10^{-10}$	0.00001
consumer	inkjet	$\$5 \times 10^{-9}$	0.0001
a-Si TFT	3 μm lithography	$\$3 \times 10^{-10}$	0.03
MOS Si	<0.1 μm lithography	$\$1 \times 10^{-11}$	3.0

It is important to consider the relative costs of patterning information over such large areas to understand the alternative routes different groups have taken to produce larger area electronics.[1,4−12] Conventional graphics printing can produce large area patterning at very low costs: <10 μcents/cm^2 and fractions of a "nanocent" per bit of printed information. In contrast, conventional thin film and wafer-based microelectronics can integrate functionality at similar or even lower costs per patterned feature at much higher resolutions in complex, highly engineered materials. However, the cost per unit area is typically much higher for conventional electronics patterning, which derives from the ability to miniaturize that has driven cost reduction in those industries. This comparison can be seen in Table 1 .

To meet the manufacturing needs for larger area electronics, numerous industrial and academic groups have endeavored, in recent years, to provide microelectronic functionality over larger areas.[13−19] It has been shown that printing can be applied to larger area electronics manufacture at various scales.[4−6,9,20,21] However, it will be a balance of costs and high functionality that will be required to make large area electronics ubiquitous in application areas spanning wireless technology, information display, energy, electronic/human interactivity, defense, and health.

In this Review, we analyze in detail the performance requirements of several large area electronics applications to capture what is needed from new materials. We review progress on efforts to create a new manufacturing industry for large area electronics by integrating printing technologies with solution-processed electronic materials. Solution-processed oxides and carbon nanotubes have been widely used in large area in the past 5 years. In this Review, however, we will concentrate on the synthesis, processing, and device performance of polymeric semiconductors.

2. Large Area Electronics Applications

In this section of the Review, we will discuss several examples that have been chosen to represent the key elements of the field. Table 2 lists some examples of the many large area electronics applications. For all of these applications, there are a range of required device and materials specifications that must be met to satisfy different applications requirements. These include critical dimensions, optoelectronic responses, and intrinsic materials and interface parameters.

2.1. Displays and Lighting

It is perhaps displays that capture the essence of large area applications most tangibly. They are large, visible, and present in ever-increasing sizes in consumer and public information display settings. Over the last several years, commonly available flat panel displays have scaled from laptop 14" diagonal screens to 40" and even >100" home theater LCD displays. Because of its commercial success and technology development rate, this industry stands as fierce competition to and an important learning model for the development of other large area semiconductor electronics applications. Furthermore, the active matrix liquid crystal displays (AMLCD) industry's ability to show cost reduction, process size scaling to $\gg$m^2 substrate areas, and maintenance of high yields with micrometer-scale features is impressive. This is a testament to the ability of a conventional, technology-driven industry's ability to evolve and improve when driven by multiple, large market demands. Conventional Si microelectronics' greatest strength has been its ability to scale device dimensions down and device densities exponentially higher, leading to low cost/function even though the cost/area can be relatively high. This is a unique feature of the evolution of the Si semiconductor industry in which process cost per unit area rises with increasing technology integration, even though cost per transistor still drops due to the even more aggressive device density scaling (ULSI integration below 50 nm can exceed 10^{14} devices/m^2). This scaling, famously tracked in time by Moore's Law,[22] has fueled monolithically integrated Si's diffusion into almost every aspect of commercial and daily activity. It is not uncommon for Moore's law to be cited incompletely, by referring to it as simply the doubling of transistors per integrated circuit every year (later modified to every 2 years). In fact, the original analysis by Moore was centered on the trend that the density of transistors at which cost per transistor was lowest would double every year. It is interesting that device density and area were just as much on Moore's mind then as it is now a concern for developers of large area electronics. However, Moore was observing Si miniaturization. For displays, this trajectory is much different. In AMLCD, it is overall display size that grows rapidly, and ultimately cost per m^2 of display that drops exponentially with new display generations as shown in Figure 1. Consider that the total device count for an AMLCD TV, typically greater than 4 M thin film transistors (TFTs) per display, is constant across increasing displays sizes. An HD 32" TV contains the same number of TFT-controlled pixels as a 50" HD TV does, but each pixel is more than twice as large. As TVs scale beyond 50", the size of a single pixel approaches 1 mm in size. In other, even larger-scale electronic display applications, such as large public information signage or advertising, devices densities of <1 device/cm^2 are easily imaginable.

In AMLCD, substrate cost has scaled up dramatically, driven, in part, by the increase in display sizes and therefore the greater number of displays that a single substrate can yield. Also, despite high tool costs and the challenging engineering of depositions, lithography, and patterning over several square meter substrate areas, the cost per square meter of display backplanes has dropped at a rate of nearly 20% per generation. Conventional photolithography-based AMLCD is on track to extend to areas approaching 100 ft^2 substrates (Gen 10) with expected yields that have not been matched by print-based deposition techniques.

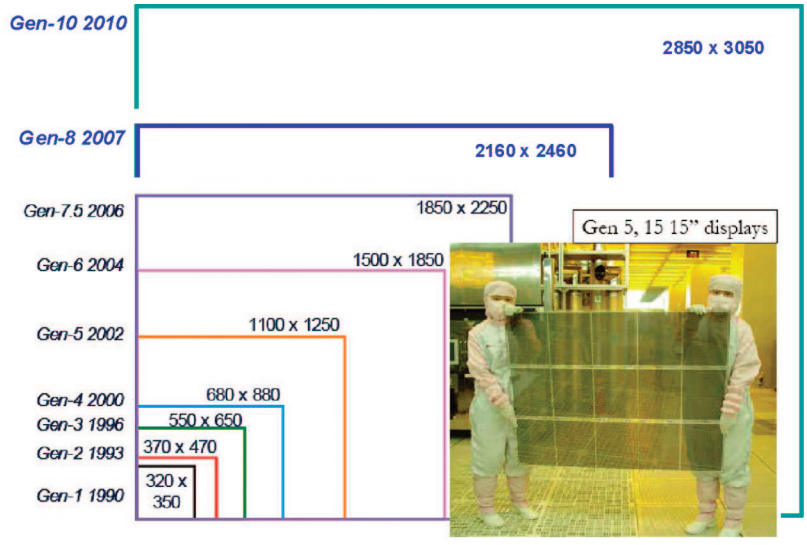
There has also been interest in pursuing novel deposition and patterning approaches to compete with or extend thin film fabrication for large area thin film semiconductor devices, and there is a theoretical case for this. As displays increase in size, the device density decreases and device placement also becomes very sparse. In this case, conventional blanket coating techniques followed by photolithography and etch are relatively inefficient in term of materials utilization and waste. There has been growing interest in novel approaches to materials deposition to increase efficiency at larger substrate areas. In the case of large area

Table 2. Examples of Large Area Electronic Applications

information displays	large reflective displays for public information and advertising based on electrophoreticmedia and larger area AMTFT backplanes
medical imaging	medical imaging arrays based on AMTFT addressed photodetectors.
lighting	OLED solid-state lighting for general and large venue illumination using large area, low-cost processing OLED displays for backlighting and advertising with large area, tin and flexible form factors
solar energy	thin film inorganic and organic photovoltaics
RF tags	RF identification tags with direct antenna integration and or reduced assembly costs RF sensor networks utilizing larger area sensor and/or antenna integration
military	military personnel and vehicle identify friend or foe indicators for nighttime identification using flexible OLED emitters larger area map displays including emissive, reflective, or semitransparent functionality flexible/conformal AMTFT reflective adaptive camouflage based on electrophoreticmedia
sensors	biochemical test matrix arrays (sensor elements and/or data addressing such as AMTFT) flexible large area sensors with integrated amplification and signal processing flexible biomedical sensors and electronics for direct body contact large pressure sensor arrays for article presence and article shape identification integrated sensing and control for integrated micro fluidics for biochemical analysis, sequencing, and micro synthesis

AMLCD, these efforts have focused on non-TFT materials such as color filter processing, polyimide deposition, and other areas.[23,24]

In new display types, such as AMOLED (active matrix organic light-emitting diode) displays, where the novel emitter materials cost can be very high, the potential benefits of local deposition techniques has driven considerable development by Epson,[25,26] Philips,[7] Cambridge Display Technology,[27]Dupont,[28] 3M,[29] Samsung,[30] Sony,[31] and others. However, there still exists a fundamental gap between the error rates and reliability issues obtained with very high accuracy print deposition and the stringent requirements of high yield displays processing (<1 ppm). This gap also extends to novel approaches for organic TFT deposition where many of the initial innovators in this area, including Plastic Logic and Philips/Polymer-Vision,[32] are currently resorting to large amounts of semiconventional processing as they work to reach acceptable manufacturing yields at introductory substrate sizes. However, the theoretical materials utilization advantages still exist for novel, local deposition



Current Display Total Cost:	$1200/m^2	($0.77/in^2)
TFT array Cost Fraction	~20-25%	($0.17/in^2)
Change in Total $ / m^2	-20% to -25%	per Generation

Figure 1. The top diagrams show the scaling of substrate glass sizes used in successive generations of active matrix liquid crystal display processing. The bottom table summarizes the cost structure and generation-to-generation reductions in cost/area.

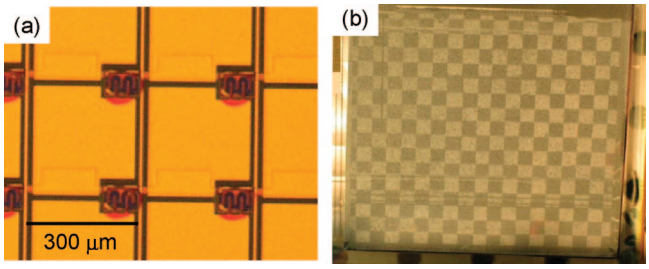


Figure 2. (a) Optical micrograph of a TFT backplane fabricated using a hybrid process where the polymer semiconductors, PQT-12, is printed and all other layers are patterned and deposited by conventional methods. (b) Image displayed by hybrid backplane when laminated with electrophoretic media from E-ink.

approaches to large area display fabrication, and many groups continue to develop materials and printing technologies to improve yield and performance.

An alternate approach for emerging large area electronics applications in displays may be to not attempt to compete with AMLCD processing in the near to midterm, but instead to focus on areas where unique value can be brought with new large area electronics processes and materials. Instead, the greatest opportunity may be to look ahead many generations to very large area display applications or in areas not competitive with current AMLCD products and that also bring some other functionality. This functionality might include flexibility, robustness in very thin form factors or ability to conform to nonplanar surfaces. Along with this very aggressive size scaling, yield issues will need to be addressed through further print or other novel process improvement, fault tolerant device and matrix designs, and testing and defect repair approaches relevant for very large area processing. Also, long-term research and development in this area should focus on the weakest links in conventional processes where print processing may also be easiest to integrate. In most current AMTFT processes, the single biggest cost, considering depreciated processing tool costs and materials costs, is typically the thin film Si deposition by CVD. Furthermore, the alignment and thickness tolerances on the semiconductor island in a large area display pixel structure can be relatively less stringent as compared to channel length definition, gate electrode placement, or OLED emitter layer thickness. Hybrid printed semiconductor approaches such as Kovio's solution-based Si,[33,34] or PARC and Polymer Vision's hybrid processes where conventional inorganic and organic processes are combined, may be interesting when extended to large areas.[5,32] In these cases, the ability to make best use of the local dispensing and materials costs savings possible with printed organics becomes attractive. A similar hybrid approach, combining printing and conventional materials deposition and etching, has also been explored by AMLCD manufacturers.[35] In Figure 2a, an optical micrograph of a hybrid TFT array is shown. The metal electrodes and bus lines are defined by photolithography, whereas the semiconductor (PQT-12) is printed from solution via inkjet printing.[5] The channel length is 10 μm, the gate dielectric is a double layer of silicon nitride and silicon oxide (deposited by PECVD), and the average TFT mobility is 0.06 cm^2/(V•s). The pixel size is 300 μm in a 160 × 180 pixel array. Figure 2b is photography of a display formed by integrating the hybrid printed backplane with electrophoretic display media from E-ink.

In the future roadmap for very large area displays, there are also new performance challenges. Consider that, as pixel

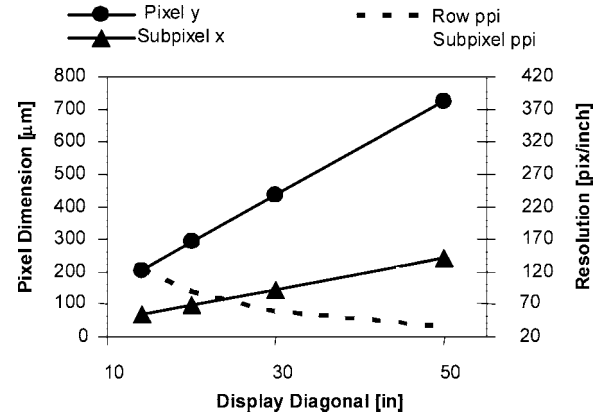


Figure 3. Relationship between pixel dimensions and display diagonal size, as the display sizes grow to current consumer TV sizes and beyond. Pixel areas become macroscopic at these large display sizes, approaching 1 mm^2 per pixel.

sizes increase above the square-millimeter dimension (see Figure 3), the pixel capacitance and leakage scale as the area of that pixel. This increase in pixel charging requirements for LCD or other reflective displays requires a corresponding quadratic increase in drive current delivered by the TFT. However, the current delivered by a TFT scales linearly with size. This means that higher TFT mobility (>1 cm^2/(V•s)) and/or low capacitance, short channel designs able to be implemented over very large areas will be required for very large LCD and reflective-type displays.

Higher TFT mobility and on-currents would also enable increased on-panel driver integration, which is another key improvement for large area and flexible AMTFT display designs. As display and interconnect length increase, the ability to perform gate row line multiplexing, panel column data drive, and more advanced display data processing is desired. Ultimately, the ability to fully integrate all driver circuitry on the display substrate is of interest, especially in the case of truly flexible and thin form factor displays where the external interconnects or the presence of mounted conventional components may also be less desirable.[36]

Typically, effective mobility of order 1 cm^2/(V•s) or higher is needed for this type of circuitry. The current in these interconnects scales with the growing pixel capacitances and required drive currents. At some critical point, concepts such as die-per-pixel drivers based on single crystal Si CMOS, such as those originally pursued by Alien Technologies[37,38] and others for smaller displays, may also be competitive. It should be noted that even for electrophoretic-type displays current demands and TFT performance will increase. Although it has been shown that small, long refresh cycle e-paper type AMTFT display can be driven with mobility of $\sim 10^{-2}$ cm^2/(V•s), larger pixel sizes, improved gray level control, and, of course, color capability will increase mobility demands toward those required for LCD.[4,6,39,40]

For novel emissive displays, such as OLED displays, the current driving requirements are extreme. Issues related to differential degradation and higher current demands for specific AMOLED colors, such as blue, put further demands on the active matrix array. Even at small sizes, stress-stable current delivery to drive OLED pixels is a challenge for amorphous silicon-based TFT technology. In contrast to AMLCD where the pixel TFTs essentially set voltages at each pixel and capacitive switching currents are of short, transient duration, AMOLEDs require continuous delivery of current to emitting OLEDs at each pixel. Unfortunately,

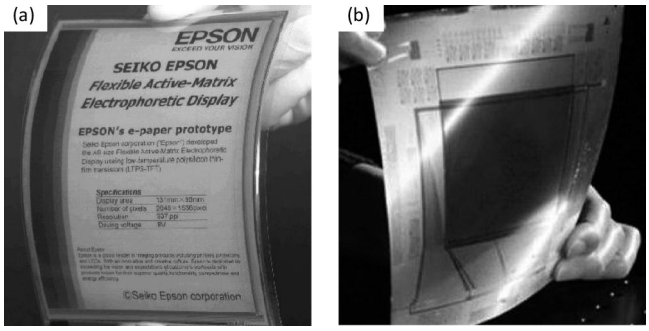


Figure 4. (a) Electrophoretic high-resolution flexible display driven by polysilicon active matrix and integrated driver circuitry (Seiko Epson). (b) A flexible polysilicon TFT array on stainless steel substrates for AMOLED drive (PARC).

amorphous silicon TFTs are susceptible to bias stress effects under sustained current drive.[41] This bias stress effect cause to threshold voltage shifts and resulting performance degradation. This leads to overall display performance degradation but also differential aging behavior for pixel of different color and utilization rates. There are circuit means to accommodate for this, and further progress in OLED efficiencies can reduce this effect. However, it remains a significant issue for long lifetime amorphous silicon (a-Si) AMOLED applications.

Commonly, polysilicon TFT technology is used for AMOLED as the higher carrier mobilities of polysilicon as compared to a-Si, and increased stability of polysilicon-based devices under bias stress, are more effective in AMOLED. However, polysilicon is typically more expensive to produce and suffers from performance variations across the TFT glass associated with the recrystallization process.[1] Polysilicon is typically produced by laser recrystallization of a-Si thin films on glass. For top emission OLED devices, there is the prospect of high temperature substrates that would allow for more uniform thermal recrystallization approaches, such as semi flexible steel.

Seiko Epson and PARC have demonstrated prototypes employing some of these novel concepts applicable to high performance thin film Si-based flexible active matrix displays.[42,43] Examples of this are shown in Figure 4a and b where photographs of a flexible high-resolution e-paper and a flexible poly silicon TFT backplane for OLEDs are displayed. Seiko Epson used a Si lift-off process to integrate the array electronics on plastic and fabricate displays, while PARC processed polysilicon TFT arrays directly on steel substrates.

Other applications of OLEDs, such as solid-state lighting, backlighting, and large area, lower information content displays, also represent future opportunities in large area electronics. In the case of general illumination, high luminance efficiency and lifetime requirements lead to a balance of performance, cost, and area. This, in turn, is balanced against the cost pressure from fluorescent lighting and emerging LED products to create a need for very low-cost, large area processing with high yield. Consider that larger area planar ~100 nm critical dimension diode technology is particularly sensitive to shorting and nonuniformities originating from process and materials defects. This includes deposited layer defects, particulates, and substrate defects. However, the growing efficiencies and lifetime for OLEDs, now exceeding 100 lm/W in laboratory demonstrations, show that the opportunity exists if the manufacturing challenges can be met.

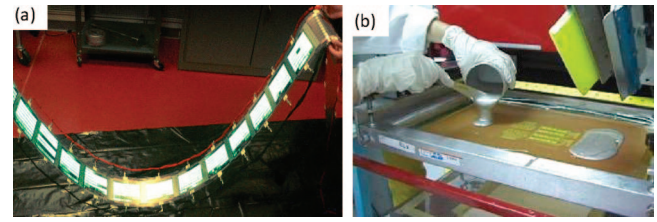


Figure 5. (a) Web-based processing of OLEDs for illumination as demonstrated by GE, and (b) Web or sheet-printable, air-stable OLED printing process demonstrated by Add-Vision.

Because of a need for robustness, thinness, and low cost, some efforts have turned to web coating and printing operations as a potential large area manufacturing solution.[44] Such large area techniques have also been applied to backlighting and low information content displays. In this, manufacturing simplicity, materials utilization, and flexible encapsulation processing are critical.[45] Examples of process research and development for large area low-cost OLEDs, including web-based demonstrations from General Electric[46] as well as the air cathode printing step used in Add-Vision's all air printed, flexible OLED process, are shown in Figure 5.[45]

2.2. Solution-Processed and Printed Large Area Photovoltaics

Many of the challenges for large area displays are shared by large area photovoltaics. Solar energy harvesting is intrinsically an area-related technology due to the finite flux of solar radiation available for collection and the efficiency limits of cell technology. In the case of thin film photovoltaics technologies, the area requirements and cost/area limits are all the more stringent, due to the lower efficiency observed in thin film cells (<8% for typical a-Si cells and ~5% for web-processable organic photovoltaics). These efficiencies dictate the need for larger collection areas to deliver the same absolute power. For example, to produce 100 W of power, thin film panels of $1-2$ m^2 in area would be required. In addition to the need for high uniformity, high throughput coating of large areas of active semiconductor absorbers, which is similar to the process challenged facing large area OLEDs for lighting, there is also a need for improved interconnect technologies. Because of the larger areas involved and a desire to minimize resistive energy losses, very low sheet resistance gridlines and interconnects, which collect charge from the cell and transport it off the cell face with minimal loss and shadowing, are required. Typically, the conductors required to achieve these goals are too thick to be deposited by evaporation or sputtering in reasonable process times. Therefore, high thickness patterned deposition techniques such as screen printing of Ag or Al pastes are often used.

Higher efficiency thin film cells, such as those based on II−VI and chalcogenide active semiconductor thin film materials, do exist and are being pursued by First Solar, Miasole, Heliovolt, Global Solar, and others. Of those, Heliovolt and Nanosolar are investigating printing and solution-based approaches to $CuInSe_2$-based thin film photovoltaics.[47] These approaches raise the possibility of achieving the high efficiencies associated with inorganic CIGS technology but with a substantially lower cost due to the novel process approach. This combination of high efficiency and low cost could lead to better cost/Watt metrics, which is central to the success of thin film photovoltaics.

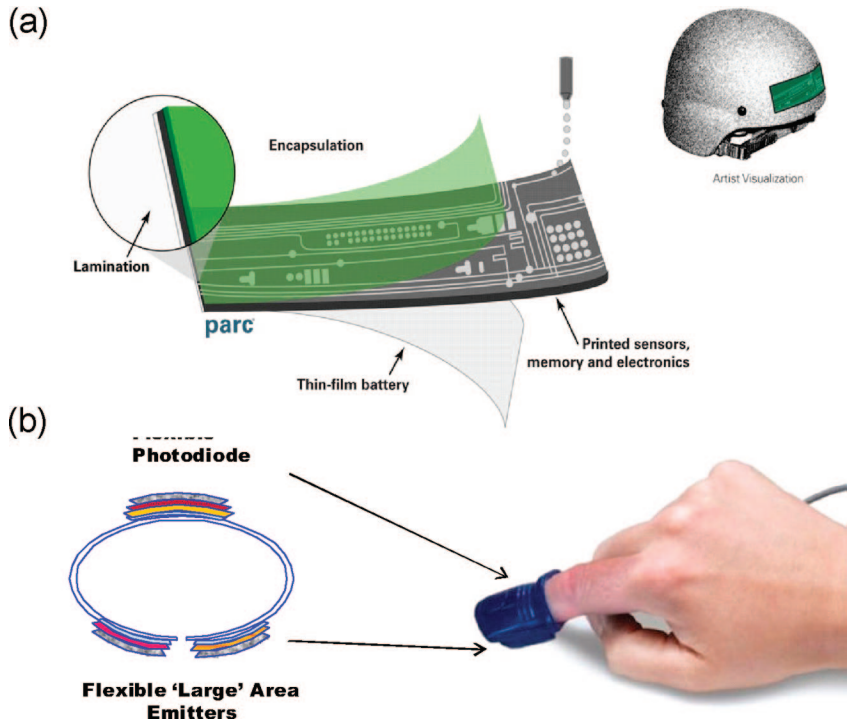


Figure 6. (a) Printed disposable blast dosimeter used to monitor events that may cause traumatic brain injury. Sensors are integrated with printed electronics and printed nonvolatile memory. (b) Direct, on-patient blood chemistry sensor concept enabled by large area, low-cost, flexible electronics.

In these cases, it is often the uniformity, stoichiometry, and multiphase homogeneity of the semiconductor active layer that represent the greatest challenges for large area scale-up of higher performing panels along with the need for a low-cost, robust encapsulation technology.[48] These parameters, in turn, directly impact yield and final cost as well as actual cell efficiency in large area and volume.

2.3. Medical Devices and Sensors

Many electronically enabled medical devices also must work at the human/electronics interface, which can be at the macroscopic length scales. This is similar to the case of displays and the nature of human vision. Interestingly, one of the first biomedical applications of large area TFT electronics in medical sensing was the X-ray image sensor array.[1,49] This array is similar to an AMLCD type TFT array except that it is an input device and does not individually address a pixelated display medium with a programmed electric field. Instead, each TFT-addressed pixel in an X-ray image sensor array is a photodiode, sensitized with a phosphor which is excited by X-rays, and is read out to scan an image.[1] The benefit of this was to replace the slow, conventional film-based X-ray process with an instantly digitized X-ray image. In this case, the large area device challenge is to realize femtoamp leakage currents and MOhm-scale on-resistances for very high-resolution TFTs.[50] The ability to have nonplanar or flexible large area arrays would allow for better signal collection around the human body with better image quality and lower X-ray doses.[19,51] Organic semiconductors are currently been used in the TFT backplane and as a photodiode in image arrays. Strain and bending studies of flexible image sensors have shown that the failure limits of organic photodiodes exceed those of a-Si.[19] However, there is also the possibility that Si CMOS technology and novel transfer processes can be combined to extend conventional Si devices into large area imaging and conformal form factors.[52]

Conformal electronics can find application in direct human sensing such as body-attached blood chemistry sensing (pulse, oxygenation, etc.). Conventional approaches to on-body pulse oximetry, for example, integrate rigid semiconductor light sources and detectors with wire attachments into clamps or bands. The cost, flexibility, and area sensitivity of the devices could be improved with large area optical sources and detectors.[53] The conventional semiconductor versions of such sensors are relatively inefficient in terms of costs and manufacturing effort investment considering that these devices, which may be able to operate for many years, are often used for relatively short periods of time and disposed of. Indeed, sterilization and reuse carry the potential drawbacks of higher costs/and or cross-contamination risks. In this sense, the conventional devices are a mismatch in terms of lifetime specification and cost. Lower cost, large area versions of these electronic products could supply better functionality in terms of flexibility, thinness, and sensitivity. In Figure 6 is shown a diagram of a noninvasive, flexible blood diagnostic application along with a diagram of a printed disposable blast dosimeter. PARC is developing a printed blast dosimeter to monitor exposure to high overpressure and acceleration that may cause traumatic brain injury. This device is designed to be used for 7 days when the data will be collected and kept as part of a person medical's history. The design includes pressure, acceleration, acoustic, and light sensors that are integrated with printed amplifiers and printed nonvolatile memory. The fact that the large area electronic devices' operating lifetimes may be shorter, which is often a challenge for emerging organic and novel thin film electronics, is not a drawback in this short product use cycle application. The use of flexible large area organic electronics in health care can also be extended to therapy enhancements such as large area emitters for photodynamic therapy.[54]

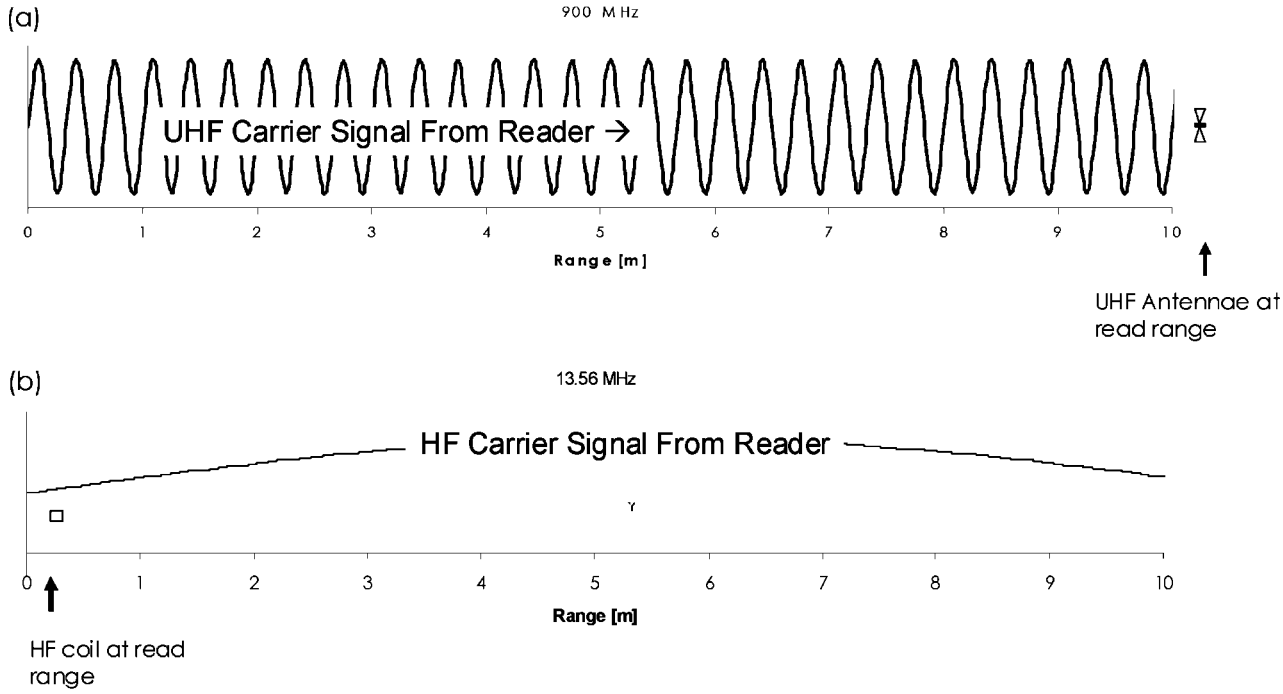


Figure 7. (a) A scaled diagram showing the relationship between UHF signal wavelength, read range, and antennae size for passive RF tag or card applications. Note that the polar antenna is of length scale similar to that of the frequency wavelength (33 cm) and reception is done in the far field through interaction with a propagating wave. (b) A similar diagram for HF 13.56 MHz operation. Note that in this case the HF coil is much smaller than the carrier wavelength and range is within the near field of the carrier signal. In this case, the area distributed RF coil that communicates with the reader interacts with an essentially homogeneous magnetic field.

There are also applications for new large area electronics approaches based on the unique optoelectronic properties of new thin film organic semiconductors in a broader range of chemical sensing electronics. Molecular Vision[55] and the contributing academic groups at Imperial College are trying to exploit microscale chemiluminescence, optical detection, and fluidic integration for new biochemical sensing applications. In one embodiment, this integrated detection system draws on the development of organic blend photodiodes based on poly(3-hexylthiophene) and [6,6]-phenyl-C61-butyric acid-methylester (PCBM), a technology that was originally developed for photovoltaic applications. The greatest future potential for sensing applications in medicine and elsewhere may lie in the direct integration of chemical sensitivity into large area device structures and materials. An example of this has been pursued by researchers at UC Berkeley where they seek to develop low-cost, high sensitivity gas sensor arrays by incorporating integrated sets of materials with complementary responses with sensory functional groups directly incorporated into the active device molecules.[56] We should also look forward to advanced large area sensing applications, which incorporate sensing and addressing electronics over large areas in highly integrated ways to further extend the human electronics interface.[10,11]

2.4. Radio Frequency Applications

In radio frequency (RF) wireless applications, the need for large area, self-powered, or maximized range device is partially driven by the fundamental physics of the frequency regimes in which they operate.[57] The governmentally controlled RF field strengths in the high frequency (HF) inductive coupling range specify the maximum energy densities available for harvesting. The HF range covers the frequency space from 3 to 30 MHz, but the primary frequency of interest for many RFID systems in this region is near 13.56 MHz due to the high carrier signal powers allowed around this frequency by regional emission regulations.[57] This puts constraints on how small an effective passive RF device can be to operate effectively in the HF range. In this context, "passive" means that the device is powered from the field itself and has no other power source. This is in contrast to "active" systems, which contain an integrated power source. Because of issues of cost and form factor, passive operation is highly desirable in applications like radio frequency identification (RFID) tags where tag cost targets are very low (<$0.05). An RFID "tag" includes an RF physical interface (i.e., antennae or coil) coupled to an RF front-end, which allows for energy harvesting and signal encoding and/or decoding between the tag and reader system that powers the tag and relays tag information to other databases or hardware. The tag also contains onboard logic circuitry, timing, and memory to enable the tag to perform its function, for example, identifying a particular item on a wharehouse pallet without contact or optical sighting. The need for large area electronics also extends to higher frequency and longer range RF frequencies where antennae length-scales need to correspond to the wavelengths of the microwave and UHF radio spectrum (typically 900 MHz and higher) and antennae dimensions are on the order of centimeters or more.

More specifically, at 13.56 MHz, a typical high frequency (HF) wireless operating frequency, inductor coil sizes on the order of square inches are required to harvest energy in the near field (see Figure 7a). This coil area requirement is also a function of the government regulated maximum RF fields at levels sufficient to drive integrated circuitry, such as passive radio frequency identification (RFID) circuits. Of course, the particular application can also place an upper requirement on the maximum size of the coil. For example, most smart card, fare card, or similar applications seek to

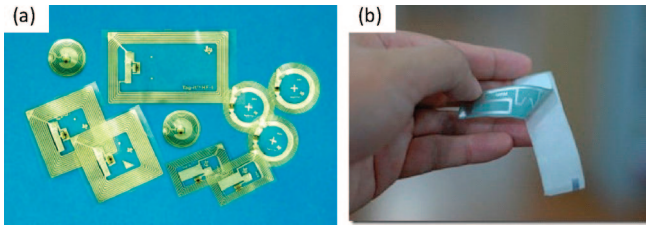


Figure 8. (a) A range of Texas Instruments 13.56 RFID tags based on etched inductive coils and attached Si chips. For size reference, the rectangular tag near the top center is the size of a credit card. (b) A UPM 900 MHz RFID label based on a dipole-type antenna and an attached Si IC chip in a label inlay format.

adhere to the ISO standard size used for bank and credit cards. For item level tagging of small products, even smaller sizes are generally sought. An ideal size would be that of a typical UPC barcode, but larger sizes, such as those of typical antitheft labels (1−3 square inches), are also of interest. See Figure 8a for some examples of Texas Instruments RFID tags based on CMOS Si and etched copper coils including "coin" tags and ISO card sizes.

In the ultra high frequency (UHF) and microwave range, coupling to the RF field typically happens in the far field at distances where the radiation is propagating as a wave. In this case, coupling to the antennae is most efficient when the antennae size is of order of the wavelength of the radiation, which would be ∼33 cm at 900 MHz. In this range, conductivity constraints on the antennae are reduced as there is not the requirement for induced current handling around a relatively long coil inductor, as was the case for HF RFID. However, due to the high frequency of the incoming signal, there is a demand for fast and low parasitic loss components to couple UHF antennae typically of order $\sim\lambda$, $\lambda/2$, or similar, and, in practice, UHF and microwave antenna layouts can often be a complex balance of directionality, power harvesting, and data bandwidth. For example, see Figure 8b.[57] As the frequency goes higher into the microwave region, there is the possibility for further antennae size reduction and even the possibility for on-chip integration of the RF antennae such as with the Hitachi μ-chip.[58] However, these typically only operate at very close range. Furthermore, the active device speeds and high directionality of communications make these applications accessible only by very high speed and low capacitance devices,[59] which may be difficult to achieve with high throughput, large area approaches.

In some cases, ease of manufacture can also be a consideration in favor of larger area processing. In conventional Si approaches to RFID, ∼1 mm^2 or smaller chips are typically attached to the antennae by conductive adhesive bond pad connections between the chip bond pads to the ≫cm^2 inductive coils or antennae. The electrical and physical attachment is made to an essentially pure metal coil (HF) or possibly a higher resistivity printed metal antennae pattern for UHF and microwave operation. The antennae cost for passive RFID tags can approach \$0.01−\$0.05 depending on size, range, and frequency response. Often an intermediate "strap" approach is used in conventional RFID assembly where the chip is attached to the ∼1 cm^2 strap, and then the strap, which contains electrical distribution traces to relatively large attachment pads on it, is subsequently connected to the antennae itself.

Highly integrated Si technology, available at standard foundries, can deliver the speed, logic, and memory functions required for high functionality RFID (typically 10^3−10^4 devices) in a very small area. Therefore, from a chip cost perspective, there is a driving force to dice a starting device wafer up into the smallest possible die size, thus yielding the most RFID devices per wafer. Currently, it is possible to realize full RFID functionality on a Si RFID chip with a die cost of <\$0.01 for a large enough scale order. However, as the device die get smaller, that is, 100s of micrometers per side, the throughput, cost, and robustness of the attach process can suffer. It is often this step that fundamentally limits RFID manufacturing throughput and cost limits as typical "pick and place" chip attach operations cost of order \$0.01−\$0.02 per attach and can require relatively slow-curing conductive adhesives. By integrating such a small Si RFID die onto an antennae, which can cost of order \$0.01−\$0.05 itself, it is possible to realize <\$0.05 RFID tags. Also, it is the attachment process that can be the focus for cost reduction.

There have been a number of research and development efforts motivated by the concept that printed active electronics could provide an alternative low-cost RF approach. The strategy is to avoid this attachment cost by directly printing the active RFID circuitry onto the antennae or vice versa. However, this approach encounters fundamental challenges. Because of encapsulation and substrate surface quality effects, the substrates required for printed electronics can be relatively expensive, and using a common substrate for the antennae and the RF circuit means that large areas of relatively high-cost substrate must be used. Furthermore, even for printed electronics, printing high functionality die over large areas leads to higher overall process costs and/or lower throughputs. On the basis of this, hybrid approaches have been proposed where intermediate size circuits, of order 1 cm^2, could be printed or processed by semiconventional thin film semiconductor processing.[60] These ∼1 cm^2 "large area" die could then be attached to antennae using relatively low resolution, high throughput, and lower cost attach processes such as simple crimping or low resolution adhesive attach. These lower resolution attach processes can cost ∼\$0.001 per attach and use higher throughput and less specialized tools.

Looking to the future, there are other large area RF applications that may also emerge such as large, locally tuned antenna arrays, wireless sensors, and ad-hoc wireless networks. For all of these new cases, the physical constraints and size mismatches seen at the various frequency ranges of RFID will be similar or even more challenging than the RFID examples given above.

In terms of device performance on the other side of the antennae, RFID tags present unique performance challenges for those developing new technology answers for this application space. Power harvesting at the carrier frequency to provide onboard power for tag operation and return communication to the reader, communication signal encoding and decoding between the tag and the reader, and logic functions on the chip are significant challenges. As shown in Figure 7, high frequency systems typically operate at 13.56 MHz, where the FCC allows higher reader broadcast powers. However, the FCC and other regulatory agencies around the world specify very tight bandwidth constraints, in part, to limit interference with other communications systems.[61] Thin film silicon and other inorganic semiconductors can produce devices operating in this frequency range. However, the very tight bandwidth specifications require very close tuning of the tag front end circuit with the reader frequency (∼1%).

The implication of this is that the tuning capacitors used in the tag, typically of order 100 pF, have to be tuned with great accuracy. This is challenging even for typically Si and passive circuitry, and there are special strategies for adjusting tag frequency response to account for manufacturing variances.

From a device speed perspective, 13.56 MHz operation seems more attractive as it is lower frequency than the 900 MHz range, which is the other major frequency of interest for high volume RFID tagging. Lower frequencies for the incoming carrier signal and lower device switching speeds do not require as short a transistor channel length, as high mobility, or as low a parasitic capacitance. All of these things favor the typically lower feature placement accuracy, larger linewidths, and lower mobilities commonly achievable with novel solution-based, printed, and large area electronics approaches. Most of the efforts toward novel thin film devices for low-cost RFID have focused in this range.[62] These efforts have shown the possibility of 13.56 MHz operational organic rectifiers. However, there is still a significant performance gap when Q-factor, off resonance tuning for higher sideband signal, and LC coil detuning during signal modulation are considered. Q-factor is a ratio between the energy stored in each wave cycle of the RF field versus the energy dissipated in each cycle through resistive and parasitic losses. Q-factors between 10 and 40 are common for RF front-end devices. There are also special timing challenges.

Because of the bandwidth limits and the defacto standard for Si devices operating in this area, timing and synchronization for 13.56 MHz RFID is done by direct division of the carrier frequency down to produce a clock signal for on-chip clock speeds. This means that, beyond the rectifier devices themselves, which are typically two terminal diodes that can have relatively short carrier transit distances across the semiconductor layer thickness, there are logical divider transistors that must also be switching directly at 13.56 MHz.[57] These devices must have very low parasitic losses (low capacitance and low on resistance). Considering all of these things and practical considerations of cutoff, frequency, logic gate switching speeds, and device geometry, it is anticipated that novel, solution-derived thin film RFID transistors for 13.56 MHz RFID operation will need: (1) TFT mobility in excess of 10 $cm^2/V \cdot s$, (2) channel lengths <5 μm,[60] (3) a self-aligned or highly accurate gate alignment process with ~ 1 μm or less overlap between transistor gate and source/drain electrodes, and (4) n- and p-type devices such that low power consumption, complementary inverters, which are the building blocks of virtually all logic, including dividers, can be implemented.[63] Some have proposed simplified timing and communication protocols to make it easier, from a tag perspective, to create a large area electronics RFID system. However, as compared to their CMOS Si-based counterparts, these simpler tag protocols typically have less functionality than their CMOS Si-based counterparts and the possibility of unresolvable multiple tag responses (called "collisions").[64]

There has been significant progress on performance of polymer semiconductors and both p- and n-type materials that present good environmental stability are now available.[65−67] The integration of p- and n-type materials enables the fabrication of complementary circuits that enhance the speed and reliability of organic-based electronics.[21,68,69] It has been shown that complete threshold voltage compensation is needed to apply complementary organic TFTs in analogue circuits.[69,70] However, if the currents and threshold voltage shifts of p- and n-type TFTs are well matched, stable digital operation is obtained.[69,70] As mentioned above, the rectifying diode is the most demanding component of a RFID tag. Pentacene-based rectifiers have been shown to operate at 50 MHz.[71] The achievement of high-frequency operation for organic rectifying diodes is a great step toward organic-based RFIDs; however, a fully integrated system that operates at 13.56 MHz remains to be obtained.

The progress on materials development and performance is due to a better understanding of the needs of each application along with the properties of the materials. Feedback on materials performance and process conditions when devices are fabricated allows chemistry groups to change the material design to achieve improved properties such as brightness, absorption range, chain packing, energy levels, solubility, and environmental stability. The next sections focus on materials that have potential to be applied to all applications described above.

3. Materials

3.1. Organic Electronics Materials

Large area, high throughput manufacturing of organic electronic products is most efficiently enabled by solution-based, additive printing techniques. This requires that the device materials can be formulated into solvent-based inks, which are then deposited by printing processes including inkjet, gravure, and flexography. In an organic transistor, the highest resolution step is usually to deposit the source and drain electrodes, whereas deposition of the dielectric and semiconductor can tolerate lower resolution techniques. The key aspect of the gate electrode patterning is that it must be precisely registered over the channel.

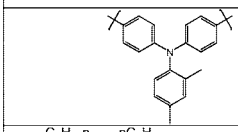
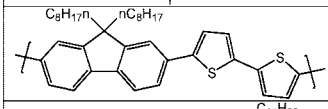
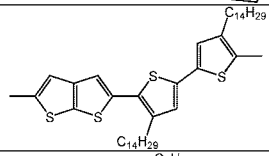
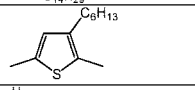
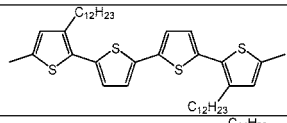
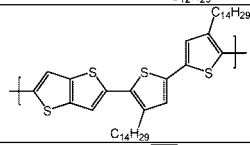
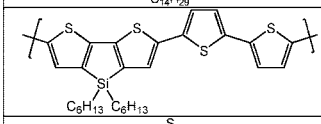
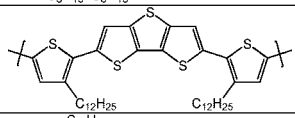
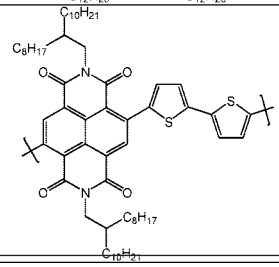
The highest value component in OLED, OTFT, and OPV devices is the organic semiconductor, and the design of new and improved semiconductor materials has been critical to the advancement of organic electronics technology. Both small molecule and polymer semiconductors can be deposited from solution, and both classes of materials are being pursued, depending on device and fabrication specifications. The highest mobility devices demonstrated in the literature have utilized small molecule semiconductors,[72] or a blend of small molecule and polymer.[73] Translating these small molecule laboratory device results into a reliable and large area manufacturing process has proven challenging. Small molecule formulations are typically low viscosity, and this can limit the processing options, which is one reason why blending with polymers approach has been developed. The crystalline domain length-scale of high mobility small molecule thin films is typically micrometers or greater, which is also the characteristic length of a transistor channel. The anisotropy of crystalline mobility, coupled with drop in mobility at grain boundaries, both contribute to large device to device variations. In applications such as OLED backplanes and large integrated circuits, performance variability from transistor to transistor cannot be tolerated. Small molecule semiconductors typically have a wide solubility parameter profile. This limits the solvents that can be used for subsequent deposition steps on top of the semiconductor film and thus also reduces the materials options. Polymer semiconductors have much smaller crystalline domains, which, over the length of a typical transistor channel, averages any anisotropy and thus reduces device to device

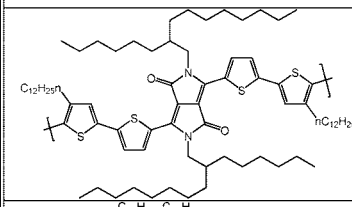
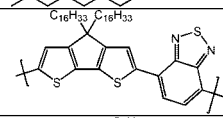
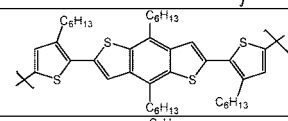
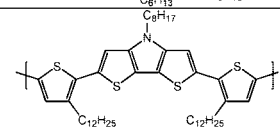
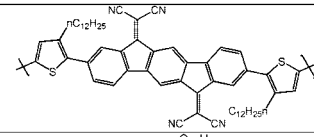
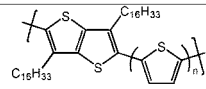
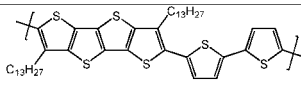
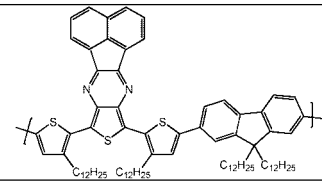
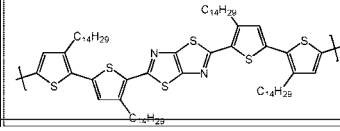
variability. Formulation viscosity in polymers can also be tailored by varying the molecular weight and even the relatively high viscosity requirements of gravure printing can be achieved with polymer semiconductors. The major challenge for high performance polymer semiconducting materials is to further improve charge carrier mobility as well as ensuring storage and operation stability. This section describes the design principles that have been employed to optimize thin film microstructure and morphology, as well providing illustrations of molecular design optimization and a state of the art review.

3.2. Semiconducting Polymer Design

Most high performing semiconducting polymers exhibit some kind of organized thin film microstructure. High charge carrier mobility is typically attributed to a coplanar conjugated backbone conformation and subsequent assembly into closely π stacked crystalline domains, often sheet-like lamellae.[74] Orientation of these domains such that the planar backbone structures are orthogonal to the plane of the substrate gives rise to the optimal charge transport.[74] As the field effect transistor device transports charge within the thin film plane and charge propagates close to the semiconductor/dielectric interface, then molecular ordering and orientation at this interface into π-stacked and aligned domains has been shown to lead to improved charge transport.[74] The polymer backbone conformation provides the molecular template from which this oriented microstructure assembles. For example, polymers containing conjugated thiophene repeat units orient such that adjacent sulfur atoms along the backbone maximize their separation by arranging in an "anti" configuration across the backbone, as shown in Table 3, and as a result 2,5 linked thiophene polymers are non rotationally invariant, with a long persistence length. Coupled thiophene units have the potential to adopt a coplanar conformation in the solid phase, allowing close intermolecular approach between adjacent backbones, stacking together in a face to face (π stacked) arrangement. Lamella structures with layers of semiconducting aromatic

Table 3. Polymer Semiconductor Structures and Reported TFT Mobility

Polymer Structure	Polymer Acronym	Charge Carrier Mobility cm^2/Vs [reference]
	PTAA	0.005 [101]
	F8T2	0.02 [9]
	pBTCT	0.1 [104]
	P3HT	0.2 [88]
	PQT	0.1 [93]
	pBTTT	0.6 [65]
	TS6T2	0.1 [109]
	PBTDT-12	0.3 [105]
	P(ND12OD-T2)	0.85 (e) [66]

Polymer Structure	Polymer Acronym	Charge Carrier Mobility cm^2/Vs [reference]
	BBTDPP1	0.1 (h) [111, 191] 0.1 (e)
	CDT-BTZ	1.4 [108]
		0.2 [95, 105]
	DTP-co-THs	0.1 [106]
	TIFDMT	0.1 (e) [113]
	pATxT	0.3 (n=1) [73] 0.2 (n=2)
	P2TDC13FT4	0.3 [112]
	ACTP-F	0.2 [114]
	PTzQT-14	0.2 [193]

backbones vertically separated by insulating layers of alkyl chains extending from the backbone can form on long-range π stacks and are vertically separated by the alkyl chains that extend from the backbone. The ability of the aliphatic layers to order into close packed structures plays a key role in influencing the domain ordering length-scale. Side-chain interdigitation between vertically adjacent lamellae has been shown to facilitate three-dimensional interlayer "registration", thus promoting large domain sizes and improved ordering.[75] This interdigitation can occur only if the side-chain attachment density along a polymer chain is low enough to permit chains from the nearest vertical lamella to occupy the free space between the chains. Regularly spaced side-chain distances are also advantageous. The side-chain density of poly(3-hexylthiophene), for example, has too high a side-chain density to permit interdigitation, whereas pBTTT, with larger spacing distance, and ordered side chains, can interdigitate,[75] leading to much larger and more ordered domains.

3.3. Poly(3-alkylthiophenes)

Regioregular (RR) poly(3-hexylthiophene) (P3HT) is an exemplary semiconducting polymer due to its ready availability, ease of processing from solution, and its promising electrical properties arising from a highly crystalline microstructure. Maximizing the regioregularity and optimizing the molecular weight[76,77] was shown to result in a systematic improvement in charge carrier mobility. The electron rich, π-conjugated, and highly planar backbone contributes to a high HOMO energy level of about -4.6 eV, and a thin film electronic absorption maximum at about 560 nm. Additional fine structure, often observed at wavelengths greater than the absorption maximum, provides a signature for aggregation.[78] This high HOMO energy level is responsible for the often observed oxidative instabilities[79] of P3HT to ambient air and humidity. When the H−T regioregularity of P3HT exceeds about 96%, charge carrier mobilities of up to 0.1 $cm^2/(V \cdot s)$ have been exhibited in an inert atmosphere.[74] The in-plane electrical properties of these crystalline films are dramatically influenced by many device and fabrication properties. For example, treatment of a bare SiO_2 dielectric surface with a hydrophobic SAM such as octyltrichlorosilane (OTS),[80] results in improved P3HT mobility and higher on-currents. A contributing factor to reduce the mobility on bare silicon oxide surface[81] is that the polar surface can "anchor" polymer chains, inhibiting large-scale self-assembly leading to faster nucleation, a less organized semiconductor microstructure, and more grain boundaries, thus lowering mobilities.

The length of the alkyl side chain also plays a role in thin film charge transport. The hexyl chain length[82,83] is reported to be optimal, with decreasing charge carrier mobility as the chain is further lengthened. As the intermolecular $\pi-\pi$ distance is similar across the different chain lengths,[84] the decrease may be due to an increase in the volume fraction of insulating side chains in the thin film. Alignment of the polymer lamellae in the plane of the substrate may be required to minimize the effect of increasing alkyl chain volume, because an in-plane percolation pathway in this orientation would not require tunnelling through insulating regions. The side-chain chemical structure has also been reported to have an effect on charge carrier mobility[84] with the conclusion that nonpolar, linear alkyl chains were optimal for backbone stacking and charge transport.

Low molecular weight, highly regioregular P3HT (~5 KDa) is highly crystalline, with a rod-like microstructure observed by AFM measurements, in which the rod width does not exceed the length of the polymer chains. Higher molecular weight P3HT (>30 KDa) with similar regioregularity is less crystalline with small nodule like crystallites. The low molecular weight films, although more crystalline, exhibit lower mobilities. It appears that the higher molecular weight P3HT has better defined and more connected grains, whereas the low molecular weight P3HT has more defined grain boundaries.[76]An enhanced out of plane twisting in low molecular weight polymer backbone conformation has also been proposed as an explanation for the difference in mobility.[77] The deviation from planarity decreases the effective conjugation length and reduces the efficiency of charge hopping. Increasing molecular weight has also been correlated with increasing crystalline quality within domains, with fewer chain ends per domain or "nanoribbon" as well as the opportunity for larger polymer chains to bridge between domains.[85] However, at high molecular weights (>~50 KDa), there is an increase in crystalline disorder, possibly due to slower crystallization kinetics. The sensitivity of P3HT microstructure to the fabrication solvent and conditions has also been observed. Higher boiling solvents promote the self-assembly of crystalline domains to occur in a longer time frame,[86] leading to improved electrical performance. More recently, this approach has been developed to demonstrate that even low regioregularity P3HT, when fabricated from very high boiling point solvents such as trichlorobenzene, can achieve high charge carrier mobilities. The solvent evaporation rate[87] was also shown to influence the polymer backbone orientation with respect to the substrate. Low evaporation rates promote the more optimal edge-on orientation. Dip coating techniques have also been utilized to fabricate highly ordered thin film layers that show mobilities up to 0.2 $cm^2/(V \cdot s)$.[88]

Chemical modification of thiophene containing backbones has been employed[89] to provide controlled manipulation of both the polymer backbone conformation and the microstructure, as well as tuning of the electronic energy levels of the molecular orbitals. For example, head to head regiopositioning of alkyl groups in adjacent thiophene units along a polythiophene leads to significant steric interactions and a resultant twist between the planes of adjacent thiophene rings. This not only reduces the π orbital overlap, but prevents a closely packed π stacked lamella microstructure, thus inhibiting crystallization. The reduced π orbital overlap significantly lowers the HOMO energy level, therefore improving ambient stability.

Alternative approaches to improve polymer ambient stability by increasing the ionization potential have incorporated electron poor comonomers such as 1,2-pyrazine[90] or perfluorobenzene[91] into the backbone. Reduction of the conjugated electron density by introduction of an electron-withdrawing group as a substituent on the polymer backbone[92] has also been employed. This serves to increase the ionization potential and can increase solubility if the appropriate functionality is used.

Polymers based on the 3,3‴-dialkyl-quaterthiophene repeat unit (PQT) were reported that could also form highly ordered thin film microstructures by self-organization through interdigitation of the solubilizing alkyl side-chains. FET charge carrier mobilities of up to 0.14 $cm^2/(V \cdot s)$ were obtained[93] on annealing within the liquid crystalline mesophase.[94] The conformational freedom of the unsubstituted bithiophene repeat unit was attributed to be responsible for reducing

effective conjugation along the backbone, leading to an increase of 0.1 eV in ionization potential over P3HT. This increase was reported to sufficiently impart an improvement in ambient stability, with transistors operating for over 1 month in ambient air.

When coupled in the 2 and 5 positions, the thieno[2,3-*b*]thiophene unit cannot form a fully conjugated pathway between coupled units. This limits the effective conjugation length that can be achieved along the backbone, with the effect of reducing the HOMO energy level and thereby increasing oxidative stability. Copolymers of thieno[3,2-*b*]thiophene with 4,4′-dialkyl-2,2′-bithiophene (pBTCT) were reported to exhibit a 0.4 eV lowering of the HOMO energy level in comparison to P3HT,[95] and transistor devices showed good stability in air, with values of up to 0.04 $cm^2/(V \cdot s)$ and corresponding on/off ratios around 10^6.

3.4. Poly(thieno(3,2-*b*)thiophenes

Poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-*b*)thiophene (pBTTT)[65] is an alternating copolymer of thieno(3,2-*b*)-thiophene and 4,4-dialkyl 2,2-bithiophene. Both monomers are centrosymmetric, and, on polymerization, the repeat unit has a rotational symmetry along the polymer long axis, which helps facilitate optimal backbone and side-chain packing, leading to a highly ordered microstructure.

The polymer was shown to orient with the backbone long axis in the plane of the substrate, and the thiophene ring plane oriented orthogonal to the substrate plane with the appropriate surface treatment. Both spectral ellipsometry and near edge X-ray absorption fine structure spectroscopy (NEXAFS) have shown[96] that, on annealing, the lamella lie in the plane of the substrate and that the backbone conjugated plane is tilted with respect to the lamella plane. The alkyl side chains also appear, from polarized IR measurements, to be well ordered in a trans configuration and are oriented tilted to the backbone. Significant side-chain interdigitation has also been identified,[75] a process that, due to the symmetry of the repeat units, can be facilitated by simple rotation round the backbone axis, unlike P3HT. Very thin films (20−30 nm thick) were observed to have micrometer size domains, spanning many polymer lengths, and a terrace like topography, in which the height of each step correlates to the cross-sectional width of the polymer backbone and tilted side chains. TEM data now suggest that these domains are comprised of clusters of nanocrystallites, although the reason that these appear to form a molecularly flat surface remains unexplained. The presence of both side-chain ordering and interdigitation are in contrast to that of regioregular P3HT, in which the side chains were concluded[97] to be "liquid like", and noninterdigitated as observed by polarized FTIR. This improved crystallinity and ordering manifests as improved charge carrier mobility. OFET devices have been fabricated from pBTTT polymer solutions, and hole mobility values of up to 0.8 $cm^2/(V \cdot s)$ were reported in a nitrogen atmosphere. These values approach that of high performing evaporated small molecule devices and are comparable to amorphous silicon.

The delocalization of electrons from the thienothiophene aromatic unit into the backbone is less favorable than from a single thiophene ring, due to the larger resonance stabilization energy of the fused ring over the single thiophene ring. This reduced delocalization along the backbone, as well as the reduced inductive electron donation from the fewer alkyl chains per repeat unit, causes a lowering of the polymer HOMO level compared to P3HT, and therefore improved ambient stability. In bottom gate, bottom contact devices, where the active semiconductor layer is exposed, the effect of different ambient conditions has been evaluated.[98,99] Exposure to unpurified, ambient air in which the humidity is approximately 50% results in an initial increase in the off current of the device. In filtered, low humidity air, transistors remain very stable over time.[99]

Further improvements in ambient stability were achieved through introduction of alkyl side chains at the 3 and 6 positions of the thieno[3,2-*b*]thiophene unit. Copolymers with both unsubstituted thiophene and bithiophene comonomers gave rise to liquid crystalline polymers with high charge carrier mobility. The bithiophene copolymer (PAT2T), for example, had a highly crystalline thin film microstructure, even as-cast, although the domain size does not approach the micrometer scale of pBTTT thin films. PAT2T has an increased ionization potential of about 0.05 eV and a hypsochromic λ max shift in the solid-state UV spectra of about 15 nm, attributed to a less planar backbone conformation. Bottom gate transistor devices exhibited charge carrier mobilities of up to 0.2 $cm^2/(V \cdot s)$ and were stable in fully ambient conditions in the dark. The monothiophene copolymer exhibited a charge carrier mobility of up to 0.3 $cm^2/(V \cdot s)$ in nitrogen.

3.5. Benchmark Polymer Semiconductors

Alkyl-substituted triphenylamine polymers (PTAA) have been shown to have excellent ambient stability.[100] The presence of the nitrogen along the backbone prevents π electron delocalization, resulting in a short conjugation length, creating low-lying HOMO energy levels and stability to oxidation. The nitrogen link is nonplanar, allows free backbone rotation, and the large linkage angle prevents π-electron stacking between backbones, leading to an amorphous microstructure and low charge carrier mobility. In top-gate device architectures, with low K dielectrics, p-type mobilities of around 0.005 $cm^2/(V \cdot s)$ were achieved with high work function electrodes.[101] As-deposited films, however, have isotropic transport and require no further heat treatment to obtain maximum mobility.

Polyfluorenes are rigid rod polymers that can be rendered soluble in organic solvents by appropriate substitution at the bridging C9 position, exhibiting high temperature liquid crystalline phases, which can be thermally exploited to achieve optimal thin film microstructures and good transistor performance.[102] The bridged phenylene units give rise to low-lying HOMO energy levels, leading to poor charge injection in FET devices from other than high work function electrodes, and subsequently poor charge transport. Incorporation of a bithiophene unit to form the alternating copolymer poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2) resulted in an increase in both HOMO energy level (from −5.8 to −5.4 eV) and improved charge transport.[103] Orientation of the polymer backbones can be achieved by a combination of thermal annealing within the mesophase and substrate induced alignment.[103] TFT mobility of up to 0.02 $cm^2/(V \cdot s)$ has been reported for this polymer, with good ambient stability.

3.6. High Performance Polymer Semiconductors

The repeat unit benzodithiophene has been incorporated into semiconducting polymer designs,[104] and when copoly-

merized with dialkylbithiophene subsequent polymers were reported to achieve mobilities of about 0.2 $cm^2/(V \cdot s)$.[105] Transistor devices also were observed to be reasonably air stable. These polymers appear to attain a self-assembled aggregated microstructure on deposition from solution, and therefore an extended thermal annealing was not required to promote good charge transport. The closely packed alkylated chain density around the backbone precludes the possibility of side-chain interdigitation, with only a high temperature main-chain melt observed on heating.

Copolymers, *N*-alkyldithienopyrrole, with alkylated thiophenes (DTP-*co*-THs) were synthesize,d[106] resulting in high charge carrier mobilities of around 0.1 $cm^2/(V \cdot s)$. Although the monomer units were shown to have a planar conformation, it was concluded that polymer thin films were amorphous, but could possess "long range π connectivity". The high electron density of the thiophene rings, coupled with the electron donation of the nitrogen on the pyrrole, contribute to a high HOMO energy level. Devices measured under argon show low on/off ratios, indicating the possibility of doping and ambient instabilities.

Copolymers of the fused monomer cyclopentabithiophene and benzothiadiazole (CDT-BTZ) were initially prepared for low band gap solar cells.[107] Nonbranched analogues with improved molecular ordering were shown to exhibit good charge transport in OFET devices.[108] Although the alkyl chains from the bridging atom project out of the plane of the planar repeat unit, extended ordering was achieved as evidenced by both the highly crystalline two-dimensional grazing incidence wide-angle X-ray diffraction patterns and the highly textured AFM images. By further purification of both monomers, higher molecular weight polymer was achieved, which was then employed in a dip-coating fabrication process to optimize molecular orientation. Very large charge carrier mobility of over 1 $cm^2/(V \cdot s)$ can be achieved in the dip-coated direction, with an approximate in-plane anisotropy of a factor of 2.

The charge carrier mobility of a copolymer of dithienosilole and bithiophene (TS6T2) was reported to reach values approaching 0.1 $cm^2/(V \cdot s)$.[109] Although the influence of the silicon atom on the molecular orbital energy level of the conjugated system is mainly to stabilize the LUMO,[110] no n-type mobility was observed. Some stabilization of the HOMO level also arises, which contributes to improved ambient air stability of these polymers in comparison to P3HT.

Exploitation of the push−pull effect of the conjugated pyrrolo[3,4-]pyrrole unit afforded ambipolar charge transport polymers where the electron donating nitrogen and withdrawing carbonyl groups create a large dipole within the fused pyrrole orthogonal to the backbone, and this effect, coupled with the planarity of the thiophene repeat units, leads to a highly aggregated, π-stacked conformation. This persisted even when the alkylthiophene monomers were coupled in a head-to-head alkyl link. With electrodes chosen to optimize charge injection, the ambipolar nature of the polymer BBTDPP1 was employed in a light-emitting transistor device.[111] Hole mobilities of around 0.1 $cm^2/(V \cdot s)$ were obtained on more standard bottom gate devices.

Extending the pBTTT design concept that has previously illustrated the beneficial effects of fused conjugated ring systems to reduce the backbone conformational freedom, a highly fused polymer tetrathienothiophene co bithiophene (P2TDC13FT4) was reported with high charge carrier mobility.[112] Although the linear alkyl side-chain incorporation density was quite low, solubility of the polymer was not a problem. Another example of high performance fused thiophene cobialkylthiophenes is the dithienothiophene analogue (PBTDT-12) of pBTTT, which was reported to exhibit mobilities of up to 0.3 $cm^2/(V \cdot s)$.[105]

The indenofluorenebis(dicyanovinylene) core unit, with the high electron-withdrawing cyano groups, was copolymerized with a tail to tail alkyl-substituted bithiophene monomer, and the resultant polymer (TIFDMT) was reported to exhibit excellent electron mobility.[113] The dicyanovinyl functionality planarizes the indenofluorene ring structure by removal of the sp^3 hybridized bridging group, which may help backbone aggregation, and indeed thin films exhibit highly crystalline textures. Electron mobilities of up to 0.16 $cm^2/(V \cdot s)$ were reported from top-contact Au electrode devices.

Acenaphtho[1,2-*b*]thieno[3,4-e]pyrazine repeat units were coupled in the 2 and 5 positions with alkylthiophene units, then copolymerized with a branched fluorene comomoner to form the polymer ACTP-F.[114] The electron-withdrawing thienopyrazine unit has a hybridized molecular orbital with the electron donation components of the conjugated polymer backbone, thus promoting a low band gap, light absorbing functionality suitable for solar cell applications. The highly planar acenaphtho[1,2-*b*]thienopyrazine unit coupled with coplanar alkyl thiophenes is likely to promote an aggregated microstructure, which promotes charge carrier mobilities of up to 0.17 $cm^2/(V \cdot s)$.

Recently a high mobility n-type polymer (P(ND12OD-T2)), with N-alkylated naphthalene diimide repeat units, was reported[66] with good ambient stability. On optimizing the device architecture, choice of dielectric, and channel length, an electron mobility of up to 0.85 $cm^2/(V \cdot s)$ was achieved, representing a significant improvement on the benchmark values for n-type polymers. The LUMO level is stabilized by the electron-withdrawing naphthalene diimide functionality, facilitating both electron injection and operational stability, while the planarity of the diimide and the bithiophene comonomers helped to promote a highly π stacked and crystalline morphology, responsible for the high charge carrier mobility. Swallow tail type alkyl chain branching from the imide functionality ensures good polymer solubility.

4. Device Stability

Most materials evaluation is done using single or a few devices, and the transition from single devices to circuits, however, is not a trivial one involving merely incremental improvements in processing technologies. To design integrated circuits with hundreds or thousands of transistors, whatever the materials and technology chosen, it is imperative to build a device model that simulates transistor behavior accurately. From the discussion in section 2, it is clear that different large area applications may require different materials. These could be low-temperature a-Si:H on flexible substrates, nano- or microcrystalline silicon, polysilicon, or more novel materials such as metal oxides, carbon nanotube mats, or organic semiconductors. One attractive feature of adapting conventional materials to large area and flexible platforms is the potential utilization of the knowledge base accumulated on materials physics, nonideal behavior, and instabilities. For instance, commercial software packages are available to simulate a-Si:H TFTs. These models are partially physics-based and take into account the transport properties of the semiconductor in addition to process-dependent fitting

parameters. Thus, the peculiarities of the I−V characteristics of low-temperature a-Si:H devices that are of interest in large area applications can be simulated with such models. Similarly, the DC characteristics of organic transistors in general obey the classic field-effect transistor (FET) equations obtained using the gradual channel approximation and therefore might lend themselves to being successfully modeled for the purpose of circuit design.[115,116] The introduction of a gate-dependent mobility is a further refinement that takes into consideration particular aspects of the charge transport physics in these materials such as multiple trapping and release of electrostatically induced charge and Poole−Frenkel effects.[117−122] While the fundamental aspects of these refinements are not completely understood, they can be introduced in device models at the phenomenological level by curve-fitting families of transfer curves. There are other nonidealities in transistor characteristics, however, that pose significant challenges to circuit designers. Electrical instability (bias stress), for example, is a progressive shift of the threshold voltage (V_T) of the transistor under operation.[123,124] Bias stress is a constant cause of concern in thin film materials of interest for large area electronics. In fact, understanding and controlling bias stress in a-Si:H films was a key step toward their application in display backplanes. The V_T shift in amorphous silicon often follows a stretched exponential law, which is attributed to the creation of trap states by the gate bias. The time-dependence of the V_T shift is well characterized in conventionally deposited a-Si:H and still being investigated in low-temperature material. In general, the V_T shifts more rapidly in a-Si:H deposited at low temperature (T < 350 °C). Recent developments, however, have produced TFTs made with low-temperature a-Si:H deposited on polyimide with stability similar to that of devices made on glass with a conventional process.[125] Long-term electrical stability remains largely unexplored in low-temperature a-Si:H on glass or flexible substrates. Even less is known about the long-term stability of emerging forms of Si such as nanocrystalline or printed films. As alternative inorganic materials to a-Si:H, mixed transition metal oxides (TMOs) containing Zn, In, and Ga have been recently investigated.[125] The electrical stability of this class of materials, which can be deposited in an amorphous or crystalline form or even printed with relatively small change in performance, is still under study. Short-term stability tests are promising and suggest that TMOs may constitute TFT channel materials capable of driving OLED displays. Thus, in light of the long-term goal of developing printed electronics, the electrical stability of printable organic transistors has become increasingly important as the carrier mobility of these materials approaches that of a-Si:H.

In addition to bias stress, other sources of nonideality are important. For instance, in a-Si:H, self-heating of short channel devices gives rise to the "kink effect", where the TFT current in saturation increases, kinking up rather than staying constant. Interestingly, the kink effect has not been observed in TMO TFTs. In organic TFTs on the other hand, as channel lengths drop below ∼10 μm the simple scaling obtained from the gradual channel approximation ($I \propto L^{-1}$, where L is the channel length) ceases to be valid. This behavior is due to the increasing importance of contact resistance at short channel lengths and to the emergence of a specific "short channel effect" in organic FETs.[126,127] Charge injection from metals into organic semiconductors is a fertile research area and is still a matter of debate.[128−132] Contact resistance models, however, reproduce device data accurately.[133] Therefore, while the contact resistance may limit device performance, it does not appear to present a fundamental impediment for device modeling and will not be discussed further here.

4.1. Bias Stress in Organic Transistors

4.1.1. Bias Stress Characterization

Bias stress depends strongly on the material, how it is processed, and the operating conditions of the transistor (i.e., biasing and environmental conditions).[134−138] Bias stress manifests itself as a decay of the output current caused by the protracted operation of the transistor. Sources of bias stress related to the presence of mobile ionic species in the dielectric are not specific to polymer semiconductor devices and will not be discussed further.[139]

It is well established that the output current decay is caused by a V_T shift during operation. The V_T shift occurs toward V_G and effectively tends to shut down the transistor. The shape of the transfer curves however does not change; therefore, the V_T shift is not due to the creation of new shallow traps but rather to charge trapping in deep traps.[123] The sheet of immobile trapped charge partially shields the gate voltage V_G, causing the current to decay at fixed V_G. Bias stress is a general phenomenon and is observed on a variety of dielectrics.[140]

In continuous bias stress experiments, a fixed V_G is applied to the transistor, and the V_T is monitored over time. If the experiment is carried on for a long enough time (typically several days), V_T approaches V_G and the time-dependence of V_T is well-approximated by a stretched exponential law:[141,142]

$$V_T(t) = V_T^0 + A\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}$$

where V_T^0 is the initial threshold voltage of the transistor, A is a constant that depends on V_G, τ is a typical relaxation time, and β is the dispersion parameter. Such kinetics are expected when charge is trapped in an exponential trap distribution having a characteristic temperature T_0.[143−145] The dispersion parameter β equals T/T_0. At times shorter than τ, the stretched exponential is approximated by a power law.[146]

Bias stress affects the extraction of transport parameters from the $I-V$ characteristics of the transistors. Hysteresis and nonideal shapes are observed when bias stress occurs at time-scales typical of device characterization (∼0.1 s to a few tens of seconds).[136] As a result, device parameters that are often used to characterize the semiconductor material appear to depend on measurement conditions. The progressive shutting off of the transistor during measurement produces a pronounced sublinear characteristic of the transfer curves and an apparent dependence of the carrier mobility on gate voltage, gate sweep rate, and dwell times. On the other hand, if the TFT is measured by starting from the on-state, the transfer curve will appear steeper and lead to an overestimate of the carrier mobility. The ideal transfer curves are recovered by making use of a pulsed gate bias, which minimizes bias stress effects during device characterization.[136]

Continuous bias measurements are useful to study the physics of bias stress. In operation, however, the transistor will be pulsed at a duty-cycle that is dictated by the application requirements. For example, in a display having

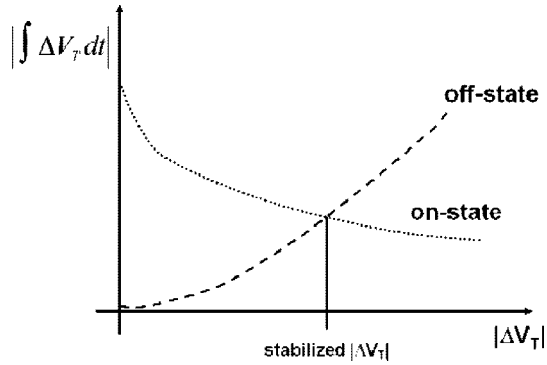


Figure 9. ΔV_T integrated during the on-cycle (on-state curve) and the off-cycle (off-state curve) as a function of V_T. ΔV_T during the on-cycle is negative, and that during the off-cycle is positive. A higher V_T implies that the device was stressed for a longer time. As the stress level increases, $|\Delta V_T|$ during the on-cycle decreases, and $|\Delta V_T|$ during the off-cycle increases. The abscissa where $|\Delta V_T|$ during the on-cycle equals that during the off-cycle is the stabilized ΔV_T.

N lines operated at a refresh rate of *R* Hz, the pixel TFT is on for 1/*NR* s and operates at a duty-cycle of 1/*N*. Differently from other disordered materials, charge trapped in organic semiconductors is partially released when the gate is turned off.[135] As a result, V_T shifts back toward its original value during the off-time of a pulsed biasing cycle. This effect is extremely important in transistors used in displays as these devices spend most of their lifetime in the off-state. Thus, during pulsed operation, the transistor eventually reaches a dynamic equilibrium state where the charge trapped during the on-cycle is released during the off-cycle and as a result the V_T remains constant (Figure 9).[125] In polythiophenes, it was observed that the elapsed time to reach stabilization, at duty-cycles in the range of 1/50 to 1/500, is about 1 day.[147] Furthermore, the stabilized V_T shift varies approximately linearly with duty-cycle.[147] Because of this dynamic equilibrium, bias stress in organic semiconductors is in actuality less severe than it may first appear by extrapolating short-term measurements, where V_T stabilization has not had time to occur yet.

Effects due to extended time (>200 days) pulsed biasing have recently been studied in polythiophenes.[148] A small decrease in V_T shift, an increase in contact resistance, and a reduction in field-effect mobility were all observed. The V_T shift reduction is in fact due to a change in the shape of the transfer and is therefore unrelated to the usual bias stress effect caused by trapping. The reduction in effective mobility, on the other hand, depends on the number of times that the transistor is switched on and off. The high transient fields occurring during switching are thought to initiate a physical degradation process of the semiconductor.[148] A possible explanation for this observation is the formation of strain in the semiconducting film caused by electrostriction.

4.1.2. Bias Stress Mechanism

While the exact bias stress mechanism is unknown, there is circumstantial evidence pointing toward several different sources of electrical instability. In polymers, bias stress rate was found to be relatively insensitive to the choice of dielectric.[136]Furthermore, release of trapped charge by band gap radiation was observed at the macroscopic and microscopic level.[136,149] As a result, it was concluded that the trapped charge is located inside the semiconductor. The initial trapping rate in polythiophenes was found to be proportional to the square of the hole concentration, suggesting the bimolecular formation of immobile bipolarons as the cause of bias stress.[150,151] The binding energy of bipolarons is strongly dependent on the local structure of the semiconductors.[152] Indeed, where charge is more localized, that is, where the semiconductor is more disordered, bipolarons are expected to have a higher binding energy due to the larger gain in backbone relaxation energy. Thus, disordered semiconductors are expected to exhibit a stronger bias stress effect than semicrystalline polymers, in agreement with experimental results observed with PQT-12 and F8T2.[153] Furthermore, the heterogeneous microstructure of semicrystalline polymers would lead to a distribution of trapping energy barriers, which would in turn lead to a power-law time-dependence of the V_T shift at long bias times, as observed experimentally.

In crystalline organic semiconductors, on the other hand, illumination with band gap radiation was found to have little or no effect on the V_T shift; therefore, the bias stress mechanism may be different. For instance, ab initio calculations suggest that the formation of hydrogen-induced traps may be responsible for bias stress in pentacene.[153]

In all cases, however, it is likely that bias stress depends on the microstructure of the semiconductor. Indeed, it has been found that single-crystal organic semiconductors can exhibit essentially negligible bias stress,[154] while evaporated thin films of the same materials display noticeable bias stress in the same conditions.[155]

Bias stress occurs in films measured in vacuum; however, its magnitude is greatly amplified by the presence of impurities. Water vapor has been recently determined to be the source of enhanced electrical instability in organic FETs, both crystalline and polymeric.[100,156−161] The trapping rate in the presence of water vapor is increased by a factor of 200 as compared to that in dry air. This effect is completely reversible: as soon as water is made to diffuse out by placing the semiconducting film in a dry environment, the transistor recovers its original bias stress behavior. Bias stress enhancement due to water was verified to be generally observed with number of semiconductors. Furthermore, analysis of the trapping kinetics demonstrated that for a wide range of microstructures, the activation energy for trapping was the same (∼0.6 eV), and therefore the wide differences in trapping rates could be attributed to the kinetic prefactor.[156] The physical origin of the prefactor is uncertain; therefore, the exact mechanism by which water molecules cause charge to be trapped at the dielectric/semiconductor interface remains unknown. Scanning probe experiments of the dielectric surface prior to semiconductor deposition showed that when a gate bias is applied, charge slowly diffuses into the channel region.[160] More hydrophobic surfaces displayed a slower charge diffusion rate, indicating that the diffusing charge is bound to surface water that adsorbs on the surface due to ambient humidity. This result is, however, in direct contrast with electric force microscopy experiments that suggested that trapping and release is much faster on OTS-treated SiO_2 surfaces, which are highly hydrophobic, than on bare SiO_2 surfaces.[162]

In addition to water vapor, a number of other vapors are found to increase the bias stress rate (e.g., acetone, mesitylene, MEK, heptane, NH_3).[163] None of the compounds analyzed caused permanent changes in the electrical characteristics of the films and were therefore only physically absorbed without forming covalent bonds. Most likely the cause of the increased bias stress rate was swelling and

general increase of the disorder in the microstructure of the film. Interestingly, in pulsed V_G measurements, the steady-state V_T was not affected by the presence of absorbed impurities in the film. Thus, the impurities greatly increase the stressing rate but simultaneously increase the detrapping rate by the same amount; they do not, however, affect the total amount of trapped charge. The formation of an intermediate state involving the trapped charge and the impurity would be consistent with this observation.

Studies of bias stress in organic TFTs indicate that the V_T shift increases strongly with charge density in the channel. Thus, there is a great advantage in operating devices at a low V_G. In most applications, the TFT footprint must be kept small, and reducing the device length is the only viable option to increase the drive current. Furthermore, as indicated in section 2, in certain applications where switching speed is crucial, short channel devices may be necessary. Nonideal behavior, however, is often observed in organic transistors with channel length shorter than approximately 10 μm, which poses challenges to the use of short channel devices.

4.2. Short Channel Effects in Organic Transistors

In attempting to optimize device performance and integrate organic thin film transistors into applications such as display backplanes and logic, a set of nonidealities arise, which make predictive device modeling and analysis increasingly difficult. The critical device parameter when reducing device size is the channel length, L. The channel length controls the maximum switching frequency, $f \propto \mu/L^2$, device integration density, $N \propto 1/L^2$, and is related to the drain current, $I_D \propto \mu/L$, which must remain high when the channel width is reduced.[164] Additionally, many organic semiconducting materials, especially those of semicrystalline or polycrystalline nature, show channel length dependence due to grain size and morphology.[72] Key performance indicators such as field effect mobility tend to increase in such materials as the channel length decreases to the order of, or smaller than, the average grain size, thus bypassing transport-hindering grain boundaries.

Nonideal device behavior due to short channel lengths is prevalent in the saturation regime. In particular, the output current is not constant in saturation, and the output current is much larger than expected based on classic device scaling leading to deviations from the square law ($I_d \propto (V_G - V_T)^2$). As a result, the effective mobility extracted from the saturation currents increases with decreasing channel length.[88,165] This effect can lead to an overestimation of the field-effect mobility by a large factor (>5). In addition, increase in off current, V_T shift, reduction in subthreshold slope, and hysteresis in device transfer characteristics have all been observed in short channel devices. Many of these effects observed in organic FETs are analogous to those previously observed and described for Si metal oxide semiconductor (MOS) FETs, despite the vast differences between organic semiconductors devices and single-crystal Si FETs. The underlying causes of these effects in MOSFETs are well understood, but the mechanisms that cause short channel effects in OFETs are under considerable debate. Nevertheless, here we outline some of the recurring short channel effects described in the literature, when they dominate, and potential approaches for mitigating some of the described nonidealities.

The morphological/structural and chemical nature of organic semiconductors is of importance when scaling device size down. When the length scale of the channel is on the order of the characteristic microstructural length-scale of the semiconductor (e.g., grain size), a dependence of the device performance on channel length is to be expected. Better performance usually results from the decrease in the number of grain boundaries present in the channel. Short channel effects, however, are observed also with glassy semiconductors and at channel lengths much larger than the grain size.[166,167] Thus, here we discuss these effects in general terms without restricting ourselves to specific semiconductors.

Channel-based effects in short channel devices occur when the ideal model for a FET begins to break down, that is, when the gradual channel approximation no longer holds. In this approximation, the electric field due to the gate voltage ($E_g = V_g/t_d$, where V_g is the gate voltage, and t_d is the dielectric thickness) is a one-dimensional function of channel position and is thus much greater than the field caused by the source drain bias ($E_{ds} = V_{ds}/L$). Interestingly, in organic TFTs, short channel effects have been observed in conditions where the electrostatics of the device are such that the gradual channel approximation should be valid (e.g., $t_d = 100$ nm, $L = 5$ μm). In these cases, however, locally near the drain contact the field becomes a two-dimensional function of position, and deviations from the ideal behavior dictated by the gradual channel approximation are detected.

In devices based on organic electronic materials, short channel effects have been observed in a variety of different materials and processing conditions. Studies used vapor deposited small molecules, such as DH4T, solution-processed polymers such as P3HT[166] and PQT-12,[165] as well as solution-processed small molecules DH4T, and *E*,*E*-2,5-bis-{40-bis-(400-methoxyphenyl)amino-styryl}-3,4-ethylenedioxy-thiophene.[167]

One of the first effects observed, as short channel effects appear in device characteristics, is channel modulation. This is observed as a lack of saturation above pinch off where $|V_g - V_T| = |V_d|$. To first approximation, this can be modeled with a constant conductance in the saturation regime: $I_{ds} = I_{ds(sat)}*(1 + \lambda V_{ds})$, where λ is the channel length modulation parameter. With a further decrease in channel length, the device characteristics at low V_{ds} are affected.

Short channel effects manifest themselves as nondestructive current punch-through. As a result, output characteristics display a severe lack of saturation, more so than channel length modulation, where the conductance is constant at saturation. In punch-through, the current shows a highly nonlinear diode-like behavior. In inorganic MOSFETs, this occurs when the source and drain depletion regions come into contact, and space charge limited current (SCLC) flows through the channel. In this geometry, the SCLC current depends on the square of the potential drop. A similar dependence is also observed in short channel OFETs, but the mechanism is not well understood. Indeed, in organic TFTs, the diode-like behavior cannot originate from depletion, because at least near the source electrode the semiconductor is accumulated. The observed behavior is, however, quite similar to that of conventional MOSFETs. In short channel ($L \approx 70$ nm) P3HT transistors, two distinct regimes were observed (Figure 10).[166] At low drain voltage, I_d is proportional to V_d, while at high bias, in saturation, I_d is proportional to V_d^n where $n = 2.4$. A power law relation with $n \sim > 2.4$ is consistent with SCLC-dominated behavior[168,169] and is in agreement with conductivity experiments of such materials in high electric fields. The diode-like dependence

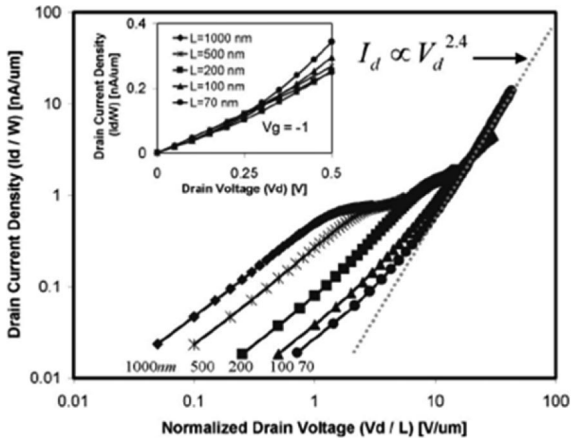


Figure 10. Output characteristics of devices with channel lengths ranging from 1 μm to 70 nm. Reprinted with permission from ref 156. Copyright 2002 AIP.

is attributed to the collection of charge carriers in the channel due to poor polymer mobility and high current densities in short channel lengths. Haddock et al., while observing a superlinear saturation behavior, only measured $n = 1.38$ under high bias, suggesting that pure SCLC behavior is not attained in their short channel devices.[167]

At longer channel length ($L = 3$ μm), the nonideal behavior is still attributed to an SCLC current. With increasing source-drain bias, a parasitic current path in the bulk of the material near the drain electrode develops, which is not controlled by the gate. Thus, the lack of saturation results from a competition between bulk and channel conductance near the drain electrode. Near pinch off, few carriers in the channel and high fields favor the bulk current. It is therefore suggested that this short channel effect is a body effect caused by semiconductor material above the channel. Transport through a device should be governed by a combination of the ideal or modified $I_{ds(sat)}$ for the channel region, and I_{sc} through the bulk, where $I_{sc} = 0.6\varepsilon\varepsilon_0\mu_b WV^2/L_b^2$, where μ_b is the mobility in the bulk of the organic semiconductor and V is voltage dropped across bulk current region L_b.[165,170] It is further suggested that while this effect takes place in all OFETs, as the channel is reduced, the contribution from L_b becomes relatively more important, and thus SCLC-dependent behavior is observed.

The most common ways to mitigate short channel effects involve altering the fields associated with the source-drain and gate biases such that the gradual channel approximation becomes valid again. One approach is to decrease the thickness of the gate dielectric to make the gate-induced field substantially larger than the transverse drain field. Indeed, device characteristics are improved and the onset of short channel effects is pushed to shorter channel lengths when the gate oxide is made thinner (from ca. 100 to 30 nm). While thinner oxides could lead to higher currents, high-k oxides and thin self-assembled monolayers dielectrics could be used to achieve even thinner equivalent oxide thicknesses, allowing for suppression of short channel effects.[167]

Other approaches attempt to cut off the bulk conductance current path that contributes to the SCLC-based punch-through effect described above. This can be obtained by making ultrathin transistors.[171] Indeed, in monolayer transistors, the typical signature of short-channel effects (mobility increasing with decreasing L) was not observed down to sub micrometer channel lenghts. Alternatively, because the electrical properties of organic semiconductors depend strongly on their microstructure, there is an opportunity to use the materials' microstructure to optimize device performance. A sequence of quenching from the melt and brief recrystallization allows the formation of a layered microstructure where a thin semicrystalline polymer layer remains at the dielectric interface while the rest of the film is disordered. As a result, the field-effect mobility remains high while the bulk mobility is decreased, thereby suppressing the parasitic SCLC component.[125]

Because of the varying nature of materials, fabrication, and device geometry, generalizations about when short channel effects begin to dominate have not been developed. The ability to model such behavior, while desirable, would require a better understanding of the mechanisms that cause these effects. At this point, it is still unclear if the multiple effects observed are all controlled by similar mechanisms, or whether a variety of factors come into play. Still, some guidelines have been set out in the literature, which can serve as a first-order predictor of these effects.[167] Short channel effects have been observed for channel lengths ranging over 2 orders of magnitude. By combining key parameters of a variety of observations in literature, short channel effects can be roughly thought to occur for channel length-oxide thickness ratios, $L/t < 20$, and longitudinal electric fields, $E_{ds} = V_{ds}/L > 10$ V/μm.[167] Specific exceptions, however, have been observed.[172] While the nature and specifics of this family of short-channel effects are still under investigation, it should be noted that they must depend on more physical quantities than only the ratio of applied fields.

5. Materials Patterning and Integration

The TFT is used as a building block for many of the applications described in section 2. Research groups focus their work on improving the performance of the TFT, improving materials synthesis for TFTs, and finding new ways of patterning these materials. One of the advantages of organic semiconductors, as shown in section 3, is that they can be processed from solution and therefore are compatible with printing techniques. A variety of printing approaches hasve been attempted to fabricate TFTs.[4−6,8,9,39,59,173−176] Each one of these techniques has different advantages and disadvantages regarding registration, process temperature, and device performance. The general approach of contact printing enables small feature sizes, but the technique tends to have poor registration accuracy for multilayer device structures.[39] Features obtained by inkjet printing are generally larger than contact printing; however, layer-to-layer registration can be very accurate.[18,177−183] The superior feature placement accuracy of inkjet printing allows gaps of 10 μm to be obtained and the source-gate overlap to be minimized.[175] The use of inkjet printing technology with sub-femtoliter droplet volume giving high-resolution features was recently reported.[21] In this work, p- and n-type organic TFTs with channel lengths as small as 1 μm were achieved. While the source/drain was the only printed layer in these devices, it is a great step toward high speed printed electronics.

Because different applications have different feature size requirements, it is not clear that a single printing technique would be used. However, it is accepted that the ultimate goal for solution-processed electronics is the development of a fabrication process that does not waste materials by depositing each layer at the same time that patterning is done. High performance, stability, and low temperature processing

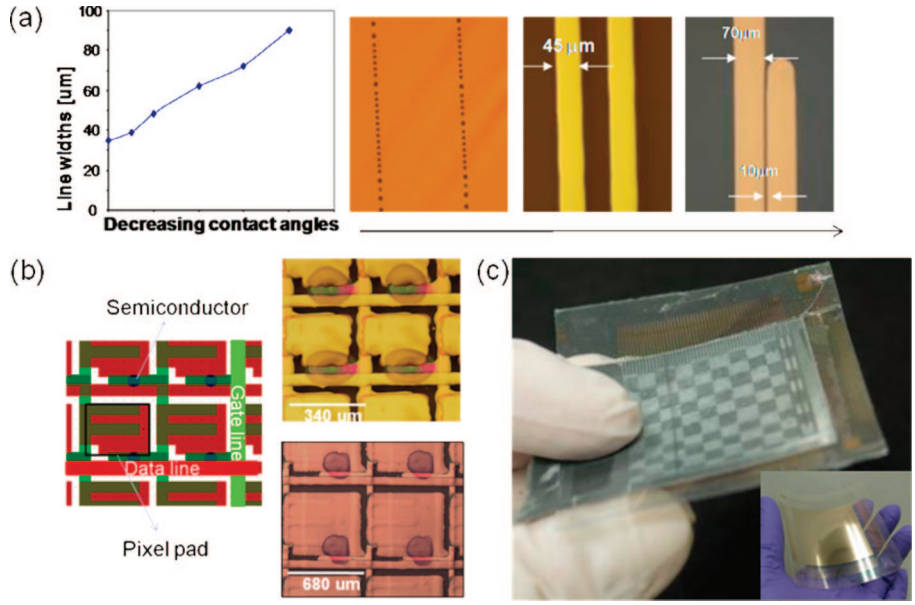


Figure 11. (a) Surface energy of gate dielectric materials is used to control the size of printed features. Disconnected drops are formed when the contact angle is higher than 80°. The printed line width can vary from 40 to 300 μm when contact angles are smaller than 75°. (b) Schematic drawing of printing file used to fabricated TFT array and optical micrographs of all printed TFT arrays with 340 and 680 μm pixel size. (c) Flexible electrophoretic display with printed active-matrix backplane. The inset shows an image of the printed array before lamination with display media. The pixel TFTs are based on the organic semiconductor PQT-12. Reprinted with permission from ref 175. Copyright 2008 SPIE Proceedings.

temperatures are also desired, as described in all sections of this Review.

One of the challenges for fabricating TFTs by printing is the control of spreading of the printed liquid inks, which ultimately defines the position and size of device components, when in contact with a solid surface. There are two competing factors when choosing the materials and solutions to be printed. It is desirable to have hydrophobic gate dielectrics to improve TFT mobility.[80] However, hydrophobic surfaces do not allow the formation of continuous printed features. In Figure 11 is displayed how an optical micrograph of disconnected drops of silver nanoparticles formed when printing was performed onto a thin film of poly(methylsilsesquioxane) (pMSSQ). The influence of water contact angle, varying from 70° to 60°, on printed line widths is shown in Figure 11a. The optical micrographs show silver lines varying from 45 and 70 μm, good edge definition (straight lines are important to define the channel length of the TFT), and gaps between features as small as 10 μm.[175] Liquid/solid interactions can also give rise to segregation of the solute to the edge of the drop or printed line; this phenomenon is known as the coffee stain effect.[184] There are several ways of controlling and avoiding the coffee stain effect. Depinning, which is often used to avoid the coffee stain effect, involves increasing contact angles, which would result in thick features and unstable printing conditions for long lines. Coffee stain effects can also be eliminated by changing the ink formulation (concentration and solvent composition) and by changing the drying conditions after printing.[175] It has been show that Marangoni flow can successfully reverse the coffee stain effect in printed drops.[4,185,186]

Once the devices are fabricated, encapsulation is required as the device characteristics such as on current and the subthreshold degrade with time once exposed to air.[98,187] The encapsulation of organic-based devices, especially thin film transistors (TFTs) using the bottom gate geometry, is not trivial because plasma deposition of inorganic layers may damage the organic semiconductor. It has been shown that phase-separated polymer−semiconductor/polymer−insulator blends can be used to pattern and encapsulate TFTs.[98] The surface energy of the gate dielectric layer is controlled to favor the segregation of the semiconductor to the channel of the TFT and induce the segregation of the polymer−insulator to the top surface. This process creates a self-assembled double layer of semiconductor/insulator where the semiconductor forms a continuous layer at the channel region of the TFT while the insulating material encapsulates the device.[98,188] Blends of components can also be used to improve the match between work function of electrodes and energy levels of semiconductors.[189] Inkjet inks formed of blends of different components are very attractive because they enable the deposition of more than one component in one step and in many cases have improved stability.

Recently, an all-additive printing process that combines metal nanoparticles, polymer dielectric, and organic semiconductors to form a flexible TFT backplane for displays was reported.[4] This process was developed at PARC over the last 5 years, and details of different steps of the process are described elsewhere.[4,5,40,175,188,190] A schematic drawing of an all printed TFT array pixel is shown in Figure 11b, where the green layers represent the gate level, the red layer is the data level, and the blue dot represents the region in the channel where the semiconductor is deposited. The potential simplicity of printed electronics is illustrated by Figure 11b, where the optical micrographs of the printed arrays match the outline of the printed file. The arrays have been integrated with E-Ink media and flexible paper-like displays are shown in Figure 11c. These types of TFT arrays are fabricated in four processing steps: deposition and patterning of gate, gate dielectric, source-drain electrodes, and semiconductor. All processing steps are additive, there is no waste of materials, and the only equipment used is an inkjet printer and an oven for sintering the silver nanoparticles and curing the gate dielectric. Careful materials choice, solvent orthogonally, and ink composition is taken into

account to stop one layer from dissolving the previously deposited material.

6. Conclusions

In conclusion, applications for large area, low-cost electronics with form factors and functionality beyond conventional Si electronics will continue to drive the growth of new emerging printed, organic, and solution-processed electronics technologies. This will require significant, closely integrated developments in materials and processing as well as a design strategy that best matches the need of the applications with the emerging capabilities of new large area electronic technologies.

It is clear that if inkjet technology is developed specifically for electronics, as opposed to document printing, high resolution will not be a limiting factor.

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